## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) ~~An active driver~~ An internal voltage generating circuit, comprising:

an internal voltage-generating unit for converting an external power supply voltage into an internal voltage according to a reference voltage and outputting the internal voltage; and

~~at least one~~ a plurality of internal voltage drop control units that are sequentially operated by ~~an~~ enable ~~signal~~ signals which are sequentially generated ~~by~~ according to ~~detecting a voltage~~ levels of the internal voltage, for stabilizing the internal voltage to a constant voltage level.

2. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 1, wherein the plurality of internal voltage drop control unit comprises:

a switching unit operated by the enable signal; and

a sub driver operated by a signal ~~to control~~ wherein the signal is also controlling the operation of an output driver of the internal voltage-generating unit, for ~~transferring~~ receiving the power supply voltage transferred through the switching unit for stabilizing the internal voltage to the constant voltage.

3. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 2, wherein the sub driver is a PMOS transistor.

4. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 1, wherein the internal voltage-generating unit is controlled so that the internal voltage-generating unit is operated according to an active signal that is generated in an active operation.

5. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 1, wherein ~~the means for generating~~ the enable signals are generated by a plurality enable signal generating units, each of the plurality of enable signal generating units comprises:

a detection unit for detecting the internal voltage according to the reference voltage;

a voltage booster unit for boosting ~~the~~ an output of the detection unit; and

an output unit for outputting the enable signal depending on ~~the~~ an output of the voltage booster unit.

6. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 5, wherein the detection unit is a current mirror that operates according to an active signal.

7. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 5, wherein the detection unit comprises:

a current mirror that operates according to an active signal; and

a stabilization unit for stabilizing ~~the~~ an output of the current mirror and outputting the output of the detection unit.

8. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 5, wherein the voltage booster unit is a level shifter.

9. (Currently Amended) The ~~active driver~~ internal voltage generating circuit as claimed in claim 5, wherein the output unit comprises:

a PMOS transistor serially connected between a power supply voltage source and a node and operated according to a power-up signal;

a first NMOS transistor connected between the node and a ground voltage source, wherein the first NMOS transistor is turned on by the output of the voltage booster unit;

a second NMOS transistor serially connected between the first NMOS transistor and the ground voltage source, wherein the second NMOS transistor is turned on by a delay signal of ~~the~~ an active signal;

a latch unit for latching the potential of the node and outputting an output signal of the latch unit; and

a NAND gate for performing a NAND operating for ~~an~~ the output signal of the latch unit, the active signal and the delay signal.

10. (New) An internal voltage generating circuit, comprising:

an internal voltage-generating unit for converting an external power supply voltage into an internal voltage according to a reference voltage and outputting the internal voltage;

a plurality of enable signal generating units for detecting a voltage level of the internal voltage and sequentially generating the enable signals; and

a plurality of internal voltage drop control units that are sequentially operated by respective enable signals, for stabilizing the internal voltage to a constant voltage level.

11. (New) The internal voltage generating circuit as claimed in claim 10, wherein the plurality of internal voltage drop control unit comprises:

a switching unit operated by the enable signal; and

a sub driver operated by a signal wherein the signal is also controlling the operation of an output driver of the internal voltage-generating unit, for receiving the power supply voltage transferred through the switching unit for stabilizing the internal voltage to the constant voltage.

12. (New) The internal voltage generating circuit as claimed in claim 11, wherein the sub driver is a PMOS transistor.

13. (New) The internal voltage generating circuit as claimed in claim 10, wherein the internal voltage-generating unit is controlled so that the internal voltage-generating unit is operated according to an active signal that is generated in an active operation.

14. (New) The internal voltage generating circuit as claimed in claim 10, wherein the plurality of enable signal generating unit comprises, respectively:

a detection unit for detecting the internal voltage according to the reference voltage;

a voltage booster unit for boosting an output of the detection unit; and

an output unit for outputting the enable signal depending on an output of the voltage booster unit.

15. (New) The internal voltage generating circuit as claimed in claim 14, wherein the detection unit is a current mirror that operates according to an active signal.

16. (New) The internal voltage generating circuit as claimed in claim 14, wherein the detection unit comprises:

a current mirror that operates according to an active signal; and

a stabilization unit for stabilizing an output of the current mirror and outputting the output of the detection unit.

17. (New) The internal voltage generating circuit as claimed in claim 14, wherein the voltage booster unit is a level shifter.

18. (New) The internal voltage generating circuit as claimed in claim 14, wherein the output unit comprises:

a PMOS transistor serially connected between a power supply voltage source and a node and operated according to a power-up signal;

a first NMOS transistor connected between the node and a ground voltage source, wherein the first NMOS transistor is turned on by the output of the voltage booster unit;

a second NMOS transistor serially connected between the first NMOS transistor and the ground voltage source, wherein the second NMOS transistor is turned on by a delay signal of an active signal;

a latch unit for latching the potential of the node and outputting an output signal of the latch unit; and

a NAND gate for performing a NAND operating for the output signal of the latch unit, the active signal and the delay signal.